IM313A

VMEbus Interface Controller V1.7

DATA SHEET

Features

- Pin-to-pin compatible with the obsolete VIC068 circuit (Cypress) with additional optimization of the external buffer control signals
- Complete VMEbus interface Controller and Arbiter
- Complete Master/slave capability
- Interleave Block transfers support
- Interrupt support
- Arbitration support
- Miscellaneous Features compliant with the VIC068A

Product Description

The IM313A is a monolithic VME controller functionally and pin-to-pin compatible with the obsolete VIC068 product. It may be used either as a direct replacement to the VIC068A in existing applications for maintenance and replications or in new developments, taking the benefit of the additional optimizations described in this document.

The IM313A provides all VMEbus system controller functions plus many other features that simplify the development of VMEbus-based modules.

Table

Design considerations

IM313A has 3 problems, to be corrected in IM313B:

- Arbiter in ROR mode: when there are 2 IM313A on VMEBUS some accesses can not be performed due to a functional misfunction between arbiter and requester in that particular mode.
- DMA, the signal BLT is wrong when local address is FE. This is linked to an internal timing problem.
- The chip is not correctly initialized if only SYSRESET is applied after power up. IRESET should also be applied after power up.

Additionally, BGIN<0..3> inputs should not be left floating when unused, as they are not internally pulled up to VCC. In the original VIC068, this recommendation also applied although some versions included integrated pull-up resistors.

IM313A is in conformity to the VME standard with two deviations to this standard.

- The first one concerns the timing number 23 which corresponds to the delay between DSA or DSB to WRITE signal in master write access (A24 D08(E0) BYTE(1), A24 D16 BYTE(0-1), A24 D16 BYTE (2-3), A16 D08(E0) BYTE(0)) . The minimum timing should be 10 ns, it is 4 ns with IM313A. This timing cannot functionally compromise the write cycle because the cycle is over on DSA/DSB rising edge.
- The second one concerns the timing number 34, which corresponds to the delay between DSA to IACKOUT in function IACK DAISY -CHAIN DRIVER. The minimum timing should be 40 ns, it is 12 ns with IM313A. This timing is sufficient to guarantee the correct operation of the cycle.

Note : - A24 means VME access where the address bus width is 24 bits.
- A16 means VME access where the address bus width is 16 bits
- D16 means VME access where the data bus width is 16 bits
- D08(EO) VME access where the data bus width is 8 bits only odd addresses

General functional description

VMEbus Interface Controller and Arbiter
- PRI, SGL, RRS arbitration
- Drive arbitration signals directly
- Arbitration timeout timer
- VMEbus timeout timer
- Drive BGOUT*, IACK* daisy-chain

VMEbus Master Interface
- Five release modes (ROR, RWD, ROC, BCAP, Release under RMC*)
- Write posting
- Indivisible cycle support
- Deadlock detection
- Fair request
- AM code generation

VMEbus Slave Interface
- Write posting
- Slave block transfer support
- Configurable local access timing

Interleaved Block Transfer support
- Block transfers with local DMA
- Programmable transfer length, burst length, interleave period and access timing
- Dual-path option

VMEbus, local Interrupt Handler/Generator includes
- Seven local interrupt signals
- Seven VMEbus interrupt signals
- Seven-level local encoding
- Error/status interrupts

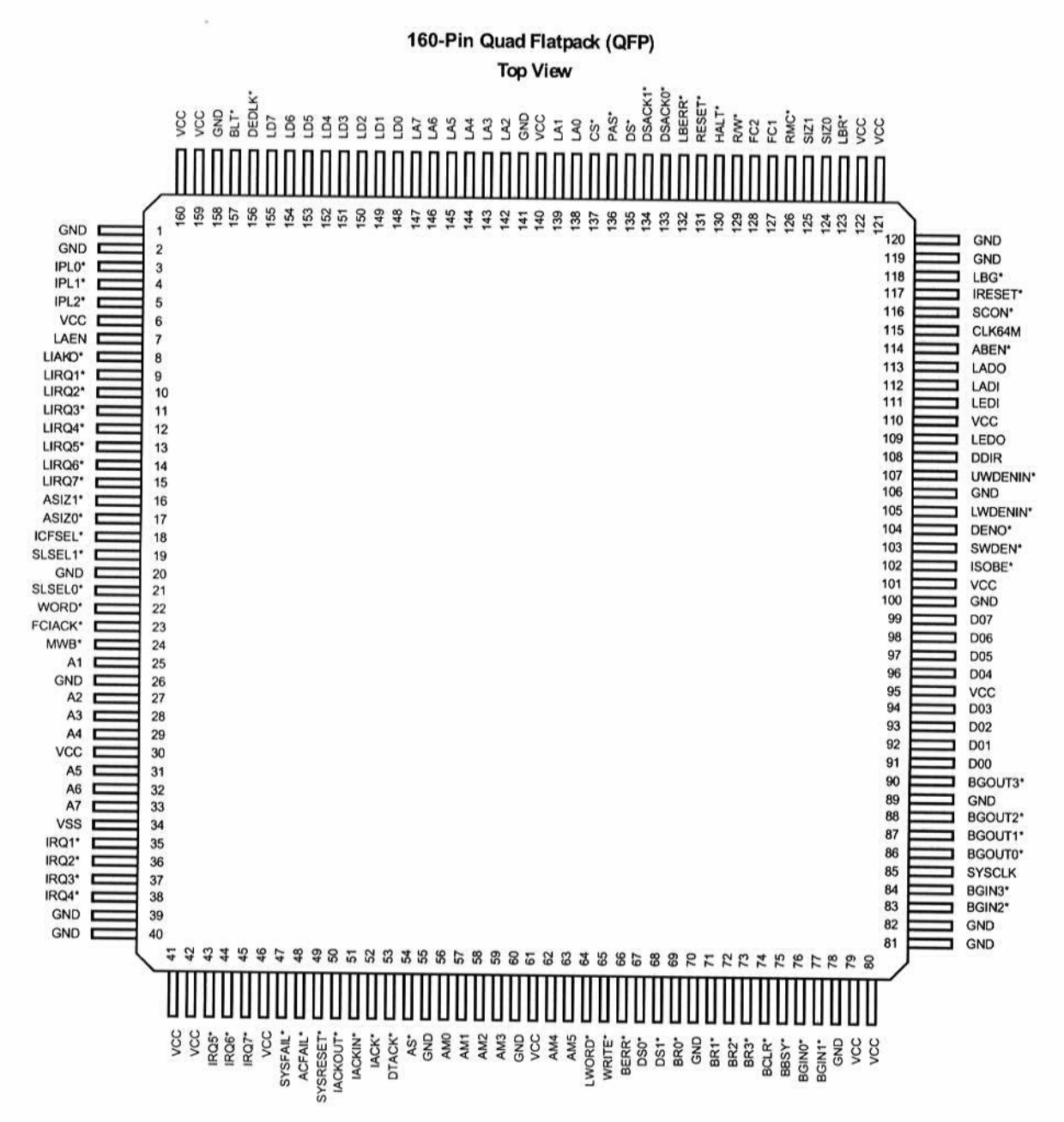
Other features included
- Local DRAM refresh control
- Local timeout timer
- “turbo” mode

I/O PORTS

QFP160 AND PGA144 pinout

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
VSS	IPL2	LIACKO*	LIRQ2*	LIRQ5*	ASIZ1	ASIZ0	SLSEL1*	WORD*	FCIACK*	A02	A04	VDD	VSS	IRQ4*	1
LD6	BLT*	IPL1	VDD	LIRQ1*	LIRQ4*	LIRQ6*	ICFSEL*	MWB*	A01	A03	A05	A07	IRQ3*	IRQ7*	2
LD2	LD5	DEDLK*	IPL0	LAEN	LIRQ3*	LIRQ7*	VSS	SLSEL0*	VSS	A06	IRQ1*	IRQ2*	IRQ6*	ACFAIL*	3
LD1	LD3	LD7	LOCATOR PIN									IRQ5*	VDD	IACKOUT*	4
LA7	LD0	LD4										SYSFAIL*	SYSRE-SET*	DTACK*	5
LA3	LA5	LA6										IACKIN*	IACK*	AM0	6
LA2	LA4	VSS										VSS	AS*	AM1	7
LA1	LA0	VCC7										VSS	AM2	AM3	8
CS*	DSACK1*	DS*										VDD	LWORD*	AM4	9
PAS*	LBERR*	RESET*										BERR*	WRITE*	AM5	10
DSACK0*	R/W*	FC1										BR2*	DS1*	DS0*	11
HALT*	RMC*	LBR*										BBSY*	BR1*	BR0*	12
FC2	SIZ0	SCON*	CLK64M	LADI	VSS	VDD	VSS8	VCC5	D00	BG1OUT*	BG2IN*	BG0IN*	BR3*	VSS	13
SIZ1	IRESET*	LADO	LEDI	DDIR	DENIN*	DENO*	D06	D03	D01	VSS7	BG0OUT*	BG3IN*	BG1IN*	BCLR*	14
LBG*	ABEN*	VDD	LEDO	DENIN1*	SWDEN*	ISOBE*	D07	D05	D04	D02	BG3OUT*	BG2OUT*	SYSCLK	VSS	15

Pin Grid Array (PGA), Bottom View


160-Pin Quad Flatpack (QFP)
Top View
1 GND
2 GND
3 IPL0*
4 IPL1*
5 IPL2*
6 VCC
7 LAEN
8 LIAKO*
9 LIRQ1*
10 LIRQ2*
11 LIRQ3*
12 LIRQ4*
13 LIRQ5*
14 LIRQ6*
15 LIRQ7*
16 ASIZ1*
17 ASIZ0*
18 ICFSEL*
19 SLSEL1*
20 GND
21 SLSEL0*
22 WORD*
23 FCIACK*
24 MWB*
25 A1
26 GND
27 A2
28 A3
29 A4
30 VCC
31 A5
32 A6
33 A7
34 VSS
35 IRQ1*
36 IRQ2*
37 IRQ3*
38 IRQ4*
39 GND
40 GND
41 VCC
42 VCC
43 IRQ5*
44 IRQ6*
45 IRQ7*
46 VCC
47 SYSFAIL*
48 ACFAIL*
49 SYSRESET*
50 IACKOUT*
51 IACKIN*
52 IACK*
53 DTACK*
54 AS*
55 GND
56 AM0
57 AM1
58 AM2
59 AM3
60 GND
61 VCC
62 AM4
63 AM5
64 LWORD*
65 WRITE*
66 BERR*
67 DS0*
68 DS1*
69 BR0*
70 GND
71 BR1*
72 BR2*
73 BR3*
74 BCLR*
75 BBSY*
76 BGIN0*
77 BGIN1*
78 GND
79 VCC
80 VCC
81 GND
82 GND
83 BGIN2*
84 BGIN3*
85 SYSCLK
86 BGOUT0*
87 BGOUT1*
88 BGOUT2*
89 GND
90 BGOUT3*
91 D00
92 D01
93 D02
94 D03
95 VCC
96 D04
97 D05
98 D06
99 D07
100 GND
101 VCC
102 ISOBE*
103 SWDEN*
104 DENO*
105 LWDENIN*
106 GND
107 UWDENIN*
108 DDIR
109 LEDO
110 VCC
111 LEDI
112 LADI
113 LADO
114 ABEN*
115 CLK64M
116 SCON*
117 IRESET*
118 LBG*
119 GND
120 GND
121 VCC
122 VCC
123 LBR*
124 SIZ0
125 SIZ1
126 RMC*
127 FC1
128 FC2
129 R/W*
130 HALT*
131 RESET*
132 LBERR*
133 DSACK0*
134 DSACK1*
135 DS*
136 PAS*
137 CS*
138 LA0
139 LA1
140 VCC
141 GND
142 LA2
143 LA3
144 LA4
145 LA5
146 LA6
147 LA7
148 LD0
149 LD1
150 LD2
151 LD3
152 LD4
153 LD5
154 LD6
155 LD7
156 DEDLK*
157 BLT*
158 GND
159 VCC
160 VCC

Nom	Pin PGA N°	Pin QFP N°	Definition	I/O type	Inputs/outputs characteristics
VCC core	G13	101	+5V Power signal	Core Power	-
VCC	D2 N1 P4 N9 J13 C15 C8	6 30 41 42 46 61 79 80 95 110 121 122 140 159 160	+5V Power signal	Power	-
VSS core	H3	20	0V Power signal	Core Power	-
VSS	K3 P1 N7 N8 R13 R15 L14 H13 F13 C7 A1	1 2 26 34 39 40 55 60 70 78 81 82 89 100 106 119 120 141 158	0V Power signal	Power	-
IPL0*	D3	3	Interrupt Priority Level 0/Global Reset	Three state I/O	Drive : 8mA
IPL1*	C2	4	Interrupt Priority Level 1	Output	Drive : 8mA
IPL2*	B1	5	Interrupt Priority Level 2	Output	Drive : 8mA
LAEN*	E3	7	Local Adress Buffer Enable	Output	Drive : 8mA
LIACKO*	C1	8	Local Interrupt Autovector	Output	Drive : 8mA
LIRQ1*	E2	9	Local Interrupt Request 1	Input	TTL Schmitt Trigger
LIRQ2*	D1	10	Interrupt Priority Level 2	Three state I/O with Pull Up	Drive : 8mA
LIRQ3*	F3	11	Local Interrupt Request 3	Input	TTL Schmitt Trigger
LIRQ4*	F2	12	Local Interrupt Request 4	Input	TTL Schmitt Trigger

Nom	Pin PGA N°	Pin QFP N°	Definition	I/O type	Inputs/outputs characteristics
LIRQ5*	E1	13	Local Interrupt Request 5	Input	TTL Schmitt Trigger
LIRQ6*	G2	14	Local Interrupt Request 6	Input	TTL Schmitt Trigger
LIRQ7*	G3	15	Local Interrupt Request 7	Input	TTL Schmitt Trigger
ASIZ1	F1	16	Address Size 1	Input	TTL Schmitt Trigger
ASIZ0	G1	17	Address Size 0	Input	TTL Schmitt Trigger
ICFSEL*	H2	18	ICF select	Input	TTL Schmitt Trigger
SLSEL1*	H1	19	Slave select 1	Input	TTL Schmitt Trigger
SLSEL0*	J3	21	Slave select 0	Input	TTL Schmitt Trigger
WORD*	J1	22	D16/D32 Control	Input	TTL Schmitt Trigger
FCIACK*	K1	23	Interrupt Acknowledge	Input	TTL Schmitt Trigger
MWB*	J2	24	Module Wants Bus	Input	TTL Schmitt Trigger
A01*	K2	25	VMEbus address	Three state I/O	Drive : 48mA
A02*	L1	27	VMEbus address	Three state I/O	Drive : 48mA
A03*	L2	28	VMEbus address	Three state I/O	Drive : 48mA
A04*	M1	29	VMEbus address	Three state I/O	Drive : 48mA
A05*	M2	31	VMEbus address	Three state I/O	Drive : 48mA
A06*	L3	32	VMEbus address	Three state I/O	Drive : 48mA
A07*	N2	33	VMEbus address	Three state I/O	Drive : 48mA
IRQ1*	M3	35	VMEbus Interupt Request	Open Collector I/O	Drive : 48mA

Nom	Pin PGA N°	Pin QFP N°	Definition	I/O type	Inputs/outputs characteristics
IRQ2*	N3	36	VMEbus Interupt Request	Open Collector I/O	Drive : 48mA
IRQ3*	P2	37	VMEbus Interupt Request	Open Collector I/O	Drive : 48mA
IRQ4*	R1	38	VMEbus Interupt Request	Open Collector I/O	Drive : 48mA
IRQ5*	N4	43	VMEbus Interupt Request	Open Collector I/O	Drive : 48mA
IRQ6*	P3	44	VMEbus Interupt Request	Open Collector I/O	Drive : 48mA
IRQ7*	R2	45	VMEbus Interupt Request	Open Collector I/O	Drive : 48mA
SYSFAIL*	N5	47	VMEbus System Fail	Open Collector I/O	Drive : 48mA
ACFAIL*	R3	48	VMEbus AC Fail	Input	TTL Schmitt Trigger
SYSRESET*	P5	49	VMEbus System Reset	Open Collector I/O	Drive : 48mA
IACKOUT*	R4	50	VMEbus Interrupt Acknowledge Output	Output	Drive : 8mA
IACKIN*	N6	51	VMEbus Interrupt Acknowledge Input	Input	TTL Schmitt Trigger
IACK*	P6	52	VMEbus Interrupt Acknowledge	Rescinding Three State I/O	Drive : 48mA
DTACK*	R5	53	VMEbus Data Transfer Acknowledge	Rescinding Three State I/O	Drive : 48mA
AS*	P7	54	VMEbus Address Strobe	Rescinding Three State I/O	Drive : 64mA
AM0*	R6	56	VMEbus Address Modifier	Three State I/O	Drive : 48mA

Nom	Pin PGA N°	Pin QFP N°	Definition	I/O type	Inputs/outputs characteristics
AM1*	R7	57	VMEbus Address Modifier	Three State I/O	Drive : 48mA
AM2*	P8	58	VMEbus Address Modifier	Three State I/O	Drive : 48mA
AM3*	R8	59	VMEbus Address Modifier	Three State I/O	Drive : 48mA
AM4*	R9	62	VMEbus Address Modifier	Three State I/O	Drive : 48mA
AM5*	R10	63	VMEbus Address Modifier	Three State I/O	Drive : 48mA
LWORD*	P9	64	VMEbus Long-Word	Rescinding Three State I/O	Drive : 48mA
WRITE*	P10	65	VMEbus Data Direction	Rescinding Three State I/O	Drive : 48mA
BERR*	N10	66	VMEbus Error	Rescinding Three State I/O	Drive : 48mA
DS0*	R11	67	VMEbus Data Strobe	Rescinding Three State I/O	Drive : 64mA
DS1*	P11	68	VMEbus Data Strobe	Rescinding Three State I/O	Drive : 64mA
BR0*	R12	69	VMEbus Request	Open Collector I/O	Drive : 48mA
BR1*	P12	71	VMEbus Request	Open Collector I/O	Drive : 48mA
BR2*	N11	72	VMEbus Request	Open Collector I/O	Drive : 48mA
BR3*	P13	73	VMEbus Request	Open Collector I/O	Drive : 48mA
BCLR*	R14	74	VMEbus Clear	Three State I/O	Drive : 64mA
BBSY*	N12	75	VMEbus Busy	Rescinding Three State I/O	Drive : 48mA

Nom	Pin PGA N°	Pin QFP N°	Definition	I/O type	Inputs/outputs characteristics
BG0IN*	N13	76	VMEbus Bus Grant Input	Input	TTL Schmitt Trigger
BG1IN*	P14	77	VMEbus Bus Grant Input	Input	TTL Schmitt Trigger
BG2IN*	M13	83	VMEbus Bus Grant Input	Input	TTL Schmitt Trigger
BG3IN*	N14	84	VMEbus Bus Grant Input	Input	TTL Schmitt Trigger
SYSCLK*	P15	85	VMEbus System Clock	Three State Output	Drive : 64mA
BG0OUT*	M14	86	VMEbus Bus Grant Output	Output	Drive : 8mA
BG1OUT*	L13	87	VMEbus Bus Grant Output	Output	Drive : 8mA
BG2OUT*	N15	88	VMEbus Bus Grant Output	Output	Drive : 8mA
BG3OUT*	M15	90	VMEbus Bus Grant Output	Output	Drive : 8mA
DO0	K13	91	VMEbus Data	Three State I/O	Drive : 48mA
DO1	K14	92	VMEbus Data	Three State I/O	Drive : 48mA
DO2	L15	93	VMEbus Data	Three State I/O	Drive : 48mA
DO3	J14	94	VMEbus Data	Three State I/O	Drive : 48mA
DO4	K15	96	VMEbus Data	Three State I/O	Drive : 48mA
DO5	J15	97	VMEbus Data	Three State I/O	Drive : 48mA
DO6	H14	98	VMEbus Data	Three State I/O	Drive : 48mA
DO7	H15	99	VMEbus Data	Three State I/O	Drive : 48mA
ISOBE*	G15	102	Isolation Buffer Enable	Output	Drive : 8mA
SWDEN*	F15	103	Swap Local Data Enable	Output	Drive : 8mA

Nom	Pin PGA N°	Pin QFP N°	Definition	I/O type	Inputs/outputs characteristics
DENO*	G14	104	VMEbus Data Buffer Enable	Output	Drive : 8mA
DENIN*	F14	105	Local Data Enable In (Lower Word)	Output	Drive : 8mA
DENIN1*	E15	107	Local Data Enable In (Upper Word)	Output	Drive : 8mA
DDIR	E14	108	Local Data Direction	Output	Drive : 8mA
LEDO	D15	109	Lacth Outgoing VMEbus Data	Output	Drive : 8mA
LEDI	D14	111	Lacth Incoming VMEbus Data	Output	Drive : 8mA
LADI	E13	112	Lacth Incoming VMEbus Address	Output	Drive : 8mA
LADO	C14	113	Lacth Outgoing VMEbus Address	Output	Drive : 8mA
ABEN	B15	114	VMEbus Address Buffer Enable	Output	Drive : 8mA
CLK64M	D13	115	64 Mhz Clock Input	Input	TTL Schmitt Trigger
SCON*	C13	116	System controller Enable	Input	TTL Schmitt Trigger
IRESET	B14	117	Internal Reset Input	Input	TTL Schmitt Trigger
LBG*	A15	118	Local Bus Grant	Input	TTL Schmitt Trigger
LBR*	C12	123	Local Bus Request	Output	Drive : 8mA
SIZ0*	B13	124	Data transfer Size 0	Rescinding Three State I/O	Drive : 8mA
SIZ1*	A14	125	Data transfer Size 1	Rescinding Three State I/O	Drive : 8mA
RMC*	B12	126	Read Modify Write	Input	TTL Schmitt Trigger

Nom	Pin PGA N°	Pin QFP N°	Definition	I/O type	Inputs/outputs characteristics
FC1	C11	127	Function Code 1	Rescinding Three State I/O	Drive : 8mA
FC2	A13	128	Function Code 2	Rescinding Three State I/O	Drive : 8mA
R/W*	B11	129	Local Data Direction	Rescinding Three State I/O	Drive : 8mA
HALT*	A12	130	Halt Status	Open Collector I/O	Drive : 8mA
RESET*	C10	131	Reset Output	Open Collector Output	Drive : 8mA
LBERR*	B10	132	Local Bus Error	Rescinding Three State I/O	Drive : 8mA
DSACK0*	A11	133	Data Size Acknowledge 0	Three State I/O	Drive : 8mA
DSACK1*	B9	134	Data Size Acknowledge 1	Three State I/O	Drive : 8mA
DS*	C9	135	Processor Data Strobe	Rescinding Three State I/O	Drive : 8mA
PAS*	A10	136	Physical/Processor Address Strobe	Rescinding Three State I/O	Drive : 8mA
CS*	A9	137	Chip Select	Input	TTL Schmitt Trigger
LA0	B8	138	Local Address	Three State I/O	Drive : 8mA
LA1	A8	139	Local Address	Three State I/O	Drive : 8mA
LA2	A7	142	Local Address	Three State I/O	Drive : 8mA
LA3	A6	143	Local Address	Three State I/O	Drive : 8mA
LA4	B7	144	Local Address	Three State I/O	Drive : 8mA
LA5	B6	145	Local Address	Three State I/O	Drive : 8mA
LA6	C6	146	Local Address	Three State I/O	Drive : 8mA
LA7	A5	147	Local Address	Three State I/O	Drive : 8mA

Nom	Pin PGA N°	Pin QFP N°	Definition	I/O type	Inputs/outputs characteristics
LD0	B5	148	Local Data	Three State I/O	Drive : 8mA
LD1	A4	149	Local Data	Three State I/O	Drive : 8mA
LD2	A3	150	Local Data	Three State I/O	Drive : 8mA
LD3	B4	151	Local Data	Three State I/O	Drive : 8mA
LD4	C5	152	Local Data	Three State I/O	Drive : 8mA
LD5	B3	153	Local Data	Three State I/O	Drive : 8mA
LD6	A2	154	Local Data	Three State I/O	Drive : 8mA
LD7	C4	155	Local Data	Three State I/O	Drive : 8mA
DEDLK*	C3	156	Deadlock Status	Output	Drive : 8mA
BLT*	B2	157	Block Transfer Status	Open Collector I/O	Drive : 8mA

FUNCTIONALITIES

System controller

When input SCON* is fixed to low level, the IM313A performs the system controller functions which are:

- priority, round-robin, or single-level arbitration
- driving IACK* daisy-chain, BGiOUT* daisy-chain, SYSCLK, SYSRESET, BCLR
- VMEbus arbitration timeout timer

Note: the SINGLE LEVEL arbitration is obtained by programming the IM313A for priority mode and programming all the VMEbus request level for all VMEbus device on the board to the same level.

Registers used in system controller functions:

- Transfer Timeout Register (TTR), bit 5-7, address A3
- Arbiter/requestor Control Register (ARCR), bit 7, address B3
- Error Group Interrupt Control Register (EGICR), bit 5, address 4B
- Bus error status register (BESR), bit 4 , address BB

Note1: In system controller mode BGiIN signals are not used, they must be tied high externally.

VMEbus Master Operations

The IM313A request the VMEbus in those cases:

- SINGLE-cycle transfer (READ, WRITE, and MASTER WRITE POSTING cycles). Those cycles are activated by the assertion of MWB* qualified by PAS*
- Indivisible Single Address Cycles (ISAC). Those cycles are activated by the assertion of RMC* qualified by PAS*. RMC* is independent of MWB* according to ICR (Interface Control Register) register bit 5, 7 programming.
- Indivisible Multiple –Address Cycles (IMAC). Those cycles are activated by the assertion of RMC* qualified by PAS*. RMC* is independent of MWB* according to ICR register bit 5, 7 programming.
- Status/ID fetch for Interrupt Acknowledge (IACK)). Those cycles are activated by the assertion of FCIACK* qualified by PAS*
- Block Transfer Requests (BLT)
- VMEBus Capture and Hold (BCAP) requests. Those requests are activated by setting the BCAP bits in the RCR (Release Control Register) register
- Self-access is signalled by asserting LBERR and BERR, and indicate this status in BESR register.
- Deadlock is signalled by asserting DEDLK*, LBERR*, HALT* according to ICR register programming.

Registers used in VMEbus Master Operations:

- Transfer Timeout Register (TTR) bits1, 2-4
- Interface Configuration Register (ICR), bits 1-7
- Arbiter/Requester Configuration Register (ARCR) bits 0-3,5,6
- Address Modifier Source Register (AMSR)
- Bus error Status Register (BESR), bits 0-3
- Slave Select 1 Control Register 0 (SS1CR0), bit 6
- Release Control Register (RCR), bits 6-7

VMEbus Slave Operations

Two signals are used to initiate slave access SLSEL0* and SLSEL1*.

Registers used in VMEbus Slave Operations:

- Slave select 0 Control Register 0 (SS0CR0), bits 0-5, address C3
- Slave select 0 Control Register 1 (SS0CR1), address C7
- Slave select 1 Control Register 0 (SS1CR0), bits 0-5, address CB
- Slave select 1 Control Register 1 (SS1CR1), address CF
- Local Bus Timing Register (LBTR), address A7
- Address Modifier Source Register (AMSR), address B7

To validate the slave access the IM313A compare the AM code received with the AMSR register. The IM313A can be configured to compare only the AM(5-3) code to AMSR(5-3) by setting AMSR(6). When AMSR(6) is set, the address size is qualified by the address size contain in the SSiCR0 (bit3-bit2) register. If both of bit3 and bit2 of SSiCR0 are set, AMSR(6) is not taken into account, AM code is compare to AMSR.

IM313A Control Register Access and Interprocessor Communication facilities

There are 58 8-bit internal registers addressable from the local bus. Among those registers, there are three categories of interprocessor communication facilities (ICFs) :

- Interprocessor Communication Registers (ICRs) : 8 8-bit registers
- Interprocessor Communication Global Switches (ICGSs) : 1 8-bit register
- Interprocessor Communication Module Switches (ICGSs) : 1 8-bit register

The signal ICFSEL* is used to access ICFs by the VMEbus master. Both local bus and VMEbus can access ICFs registers. The others registers can only be accessed by local bus. The IM313A check the AM code input to validate the access and it checks the A(5-1) address inputs to select the register.

To access registers by local bus, CS*, PAS* and DS* are driven low. Decoding SIZ1/SIZ0 and LA(1-0) validates the register access. Even if address are given with LA(1-0) = 11 in the specification, address with LA(1-0) = 00 is the same if it is a long word access (SIZ1, SIZ0 = 00).

The register **ICR5** (Interprocessor Communication Register n°5) contains the IM313A version register that is "**FE**" in hexadecimal for version number 14.

Table1: Register Values after Reset Operations

Address (hex)	Name	Description	Global Reset	Internal Reset	System Reset
03	VIICR	VMEbus Interrupter Interrupt Control Register	11111000	11111***	11111***
07-1F	CICR1-7	VMEbus Interrupt Control Registers 1-7	11111000	11111***	11111***
23	DMASR	DMA Status Register	11111000	11111***	11111***
27-3F	LICR1-7	Local Interrupt Control Registers 1-7	1000X000	1***X***	1***X***
43	ICGSICR	ICGS Interrupt Control Register	11111000	11111***	11111***
47	ICMSICR	ICMS Interrupt Control Register	11111000	11111***	11111***
4B	EGICR	Error Group Interrupt Control Register	1111X000	1111X***	1111X***
4F	ICGSVBR	ICGS Vector Base Register	000011XX	000011XX	000011XX
53	ICMSVBR	ICMS Vector Base Register	000011XX	000011XX	000011XX
57	LIVBR	Local Interrupt Vector Base Register	00001XXX	00001XXX	00001XXX
5B	EGIVBR	Error Group Interrupt Vector Base Register	00001XXX	00001XXX	00001XXX

5F	ICSR	Interprocessor Communications Switch Register	00000000	****0000	00000000
63–73	ICR0-4	Interprocessor Communications Registers 0–4	00000000	00000000	00000000
77	**ICR5**	Interprocessor Communications Register 5	**11111110**	**11111110**	**11111110**
7B	ICR6	Interprocessor Communications Register 6	X11111XX	X1111111	X1111110
7F	ICR7	Interprocessor Communications Register 7	00X00000	*0XX****	00X00000
83	VIRSR	VMEbus Interrupt Request Status Register	00000000	*******0	00000000
87–9F	VIVBR 1–7	VMEbus Interrupt Vector Base Registers 1–7	00001111	********	00001111
A3	TTR	Transfer Timeout Register	01101000	01101000	01101000
A7	LBTR	Local Bus Timing Register	00000000	********	********
AB	BTDR	Block Transfer Definition Register	11110000	11110000	11110000
AF	ICR	Interface Configuration Register	0000000X	0000000X	0000000X
B3	ARCR	Arbiter/Requester Configuration Register	01100000	011*0000	011*0000
B7	AMSR	Address Modifier Source Register	00000000	00000000	00000000
BB	BESR	Bus Error Status Register	X0000000	X0000000	X0000000
BF	DMASR	DMA Status Register	00000000	00000000	00000000
C3	SS0CR0	Slave Select 0 Control Register 0	00000000	00******	00******
C7	SS0CR1	Slave Select 0 Control Register 1	00000000	********	********
CB	SS1CR0	Slave Select 1 Control Register 0	00000000	00******	00******
CF	SS1CR1	Slave Select 1 Control Register 1	00000000	********	********
D3	RCR	Release Control Register	00000000	00000000	00000000
D7	BTCR	Block Transfer Control Register	00000000	00000000	00000000
DB	BTLR1	Block Transfer Length Register 1	00000000	00000000	00000000
DF	BTLR0	Block Transfer Length Register 0	00000000	00000000	00000000
E3	SRR	System Reset Register	11111111	11111111	11111111
EB-FF		Reserved Locations	11111111	11111111	11111111

VMEbus Interrupter Interrupt Control Register

Name: VIICR
Address: $03
Description: Provides enabling and IPL level encoding for the local interrupt issued when a VMEbus interrupt is acknowledged.
Bits 2–0: IPL value. Value is inverted and driven onto the IPL lines when an interrupt is acknowledged
Bits 6–3: Undefined/Reserved. Bits will read as 1s.
Bit 7: VMEbus interrupt mask. When clear, the IM313A signals a local in-terrupt at the acknowledgment of a previously issued VMEbus interrupt. When set, the IM313A will not issue a local interrupt.

VMEbus Interrupt Control Registers 1–7

Name: VICR1–7
Addresses: $07, $0B, $0F, $13, $17, $1B, $1F For Interrupts: 1 2 3 4 5 6 7
Description: Provides enabling of the IM313A as VMEbus interrupt handler for any or all of the VMEbus interrupts. Seven registers exist to provide unique masking and IPL values for the seven VMEbus interrupts.
Bits 2–0: IPL value. Value is inverted and driven onto the IPL signals when a VMEbus interrupt is acknowledged.
Bits 6–3: Undefined/Reserved. Bits will read as 1s.
Bit 7: VMEbus interrupt mask. When clear, the IM313A acts as a VMEbus interrupt handler by signaling a local interrupt at the specified IPL level. When set, the IM313A does not handle the VMEbus interrupt and no local interrupt is issued.

DMA Status Interrupt Control Register

Name: DMASICR
Address: $23
Description: Provides enabling and IPL-level encoding for the DMA-complete inter-rupt issued by the IM313A when any IM313A local DMA operation completes (successfully or unsuccessfully).
Bits 2–0: IPL value. Value is inverted and driven onto the IPL lines when interrupt is acknowledged.
Bits 6–3: Undefined/Reserved. Bits will read as 1s.
Bit 7: DMA status interrupt mask. When clear, the IM313A signals a local interrupt at the completion of any IM313A local DMA operation. When set the IM313A will not issue a local interrupt.

Local Interrupt Control Registers 1–7

Name: LICR1–7
Address: $27, $2B, $2F, $33, $37, $3B, $3F For LIRQ: 1 2 3 4 5 6 7
Description: Provides enabling, IPL level, and control of local interrupts 1–7 (LIRQ1–7*).
Bits 2–0: IPL value. Value is inverted and driven onto the IPL lines when a local interrupt is presented on the LIRQ1–7* signals and bit 7 of this register is clear (enabled).

Bit 3: LIRQ1–7* voltage state. A cleared bit indicates the LIRQ1–7* signal is asserted at the IM313A.
Bit 4: Auto vector enable. When set, the IM313A will supply the interrupt status/ID vector for the local interrupt acknowledge cycle. When cleared, the IM313A will assert the LIACK0* signal to indicate an 68K "auto vector" condition or that the interrupting source should provide the Status/ID vector to the processor.
Bit 5: Edge/level enable. When cleared, the IM313A responds to the LIRQ1-7* as a level sensitive interrupt. When set, the IM313A responds to LIRQ1–7* as an edge sensitive interrupt.
Bit 6: Polarity set. When set, the IM313A responds to interrupts as active High if bit 5 is clear (level sensitive) or on a rising edge if bit 5 is set (edge sensitive). When clear, the IM313A responds to interrupts as active Low if bit 5 is clear (level sensitive) or on a falling edge if bit 5 is set (edge sensitive).
Bit 7: Local interrupt mask. When clear, the IM313A is enabled to handle the corresponding local interrupt asserted on the LIRQ1–7* signals.

ICGS Interrupt Control Register

Name: ICGSICR
Address: $43
Description: Provides enabling and IPL encoding for the four global switch interrupts.
Bits 2–0: IPL Value. Value is inverted and driven onto the IPL signals when a global switch is acknowledged.
Bit 3: Undefined/Reserved. Bit will read as a 1.
Bit 4: ICGS0 mask. When clear, the IM313A will issue and handle a local interrupt when global switch 0 is set.
Bit 5: ICGS1 mask. When clear, the IM313A will issue and handle a local interrupt when global switch 1 is set.
Bit 6: ICGS2 mask. When clear, the IM313A will issue and handle a local interrupt when global switch 2 is set.
Bit 7: ICGS3 mask. When clear, the IM313A will issue and handle a local interrupt when global switch 3 is set.

ICMS Interrupt Control Register

Name: ICMSICR
Address: $47
Description: Provides enabling and IPL encoding for the four module switch interrupts.
Bits 2–0: IPL Value. Value is inverted and driven onto the IPL signals when a module switch is acknowledged.
Bit 3: Undefined/Reserved. Bit will read as a 1.
Bit 4: ICMS0 mask. When clear, the IM313A will issue and handle a local interrupt when module switch 0 is set.
Bit 5: ICMS1 mask. When clear, the IM313A will issue and handle a local interrupt when module switch 1 is set.
Bit 6: ICMS2 mask. When clear, the IM313A will issue and handle a local interrupt when module switch 2 is set.
Bit 7: ICMS3 mask. When clear, the IM313A will issue and handle a local interrupt when module switch 3 is set.

Error-Group Interrupt Control Register

Name: EGICR
Address: $4B
Description: Provides enabling and IPL encoding for the error group interrupts.
Bits 2–0: IPL Value. Value is inverted and driven onto the IPL signals when an error group interrupt is acknowledged.
Bit 3: SYSFAIL* asserted. This bit is set whenever SYSFAIL* is detected asserted.
Bit 4: SYSFAIL* interrupt mask. When clear, the IM313A generates a local interrupt when SYSFAIL* is asserted.
Bit 5: Arbitration timeout interrupt mask. When clear, the IM313A generates a local interrupt when an arbitration timeout has occurred.
Bit 6: Write post fail interrupt mask. When clear, the IM313A generates a local interrupt when a write post operation has failed due to a bus error. For master write posts, an assertion of BERR* will trigger an interrupt. For slave write posts, an assertion of LBERR* will trigger an interrupt.
Bit 7: AC Fail interrupt mask. When clear, the IM313A generates a local interrupt when ACFAIL* is detected as asserted.

ICGS Interrupt Vector Base Register

Name: ICGSIVBR
Address: $4F
Description: Provides the status/ID vector for the global switch interrupts. This register must be written after any IM313A reset to enable identification encoding for bits 1-0.
Bits 1–0: Global switch number (read-only). This value indicates which global switch is pending during a global switch interrupt acknowledge cycle. These bits are used with bits 7–2 to provide a unique status/ID vector for each global switch. The numeric value of this field indicates the switch number. These bits are valid only during the interrupt acknowledge cycle.
Bits 7–2: Status/ID. These bits are user-definable and are used with bits 1–0 to provide a unique global switch interrupt status/ID vector.

ICMS Interrupt Vector Base Register

Name: ICMSIVBR
Address: $53
Description: Provides the status/ID vector for the module switch interrupts. This register must be written after any IM313A reset to enable identification encoding for bits 1-0. This register is reset to $F0 during any IM313A reset.
Bits 1–0: Module switch number (read-only). This value indicates which module switch is pending during a module switch interrupt acknowledge cycle. These bits are used with bits 7–2 to provide a unique status/ID vector for each module switch. The numeric value of this field indicates the switch number. These bits are valid only during the interrupt acknowledge cycle.
Bits 7–2: Status/ID. These bits are user-definable and are used with bits 1–0 to provide a unique module switch interrupt status/ID vector.

Local Interrupt Vector Base Register

Name: LIVBR
Address: $57
Description: Provides the status/ID vector for the local interrupts. This register must be written after any IM313A reset to enable identification encoding for bits 2–0. This register is reset to $F0 during any IM313A reset.
Bits 2–0: Local Interrupt number (read-only). This value indicates which local interrupt is pending during a local interrupt acknowledge cycle. These bits are used with bits 7–3 to provide a unique status/ID vector for each local interrupt. The numeric value of this field indicates the local interrupt number. These bits are valid only during the interrupt acknowledge cycle.
Bits 7–3: Status/ID. These bits are user-definable and are used with bits 1–0 to provide a unique local interrupt status/ID vector.

Error Group Interrupt Vector Base Register

Name: EGIVBR
Address: $5B
Description: Provides the status/ID vector for the error group interrupts. This register must be written after any IM313A reset to enable identification en-coding for bits 2–0. This register is reset to $F0 during any IM313A reset.
Bits 2–0: Error/Status Group Interrupt number (read-only). This value indicates which group interrupt is pending during the interrupt acknowledge cycle. These bits are used with bits 7–3 to provide a unique status/ID vector for each error group interrupt. These bits are valid only during the interrupt acknowledge cycle.

Bits 2–0	Error/Status Interrupt
000	ACFAIL* asserted
001	Write post failed
010	Arbitration timeout
011	SYSFAIL* asserted
100	VMEbus Interrupter interrupt acknowledge
101	DMA complete

Bits 7–3: Status/ID. These bits are user-definable and are used with bits 1-0 to provide a unique interrupt status/ID vector.

Interprocessor Communications Switch Register

Name: ICFSR
Address: $5F
Description: Provides setting, clearing, and monitoring of the interprocessor switch interrupts via the local bus. If the switch interrupts are enabled, setting these bits (more precisely, a clear-to-set transition) causes a local interrupt to occur in the same way as if the switch was set over the VMEbus.
Bits 3–0: Module switches. Bits 0, 1, 2, and 3 correspond to ICMSs 0, 1, 2, and 3 respectively.

Bits 7–4: Global switches. Bits 4, 5, 6, and 7 correspond to ICGSs 0, 1, 2, and 3 respectively.

Interprocessor Communication Registers 0–4

Name: ICR0–4
Addresses: $63, $67, $6B, $6F, $73 For registers: 0 1 2 3 4
Description: These are general-purpose read/write registers that can be accessed from either the local bus or the VMEbus. The addresses listed above are the local addresses.
Bits 7–0: Data field.

Interprocessor Communication Register 5

Name: ICR5
Address: $77
Description: This register provides the IM313A version/revision number.
Bits 7–0: IM313A version/revision (read-only).

Interprocessor Communication Register 6

Name: ICR6
Address: $7B
Description: This register provides local or remote reset and HALT*. The address listed above is the local address.
Bits 1–0: Reset/HALT* status (read-only from VMEbus). These bits provide reset/HALT* status of the IM313A and local resources according to the following table:

Bits 1–0	Reset/HALT* Status
01	HALT* has been asserted longer than 6 ms by a source other then the IM313A. These bits may both be reset by the local CPU to indicate local resources are running and operational
10	The IM313A has performed a local reset function and the IM313A is not the system controller. These bits may both be reset by the local CPU to indicate local resources are running and operational
11	Indicates that the CPU has just been released from a system
00	Local resources are running and operational. This pattern must be written by the local CPU after a reset condition to indicate that local resources are running and operational

Bits 5–2: Undefined/Reserved. Bits will read as 1s.
Bit 6: IRESET* and HALT* status (read-only from VMEbus). This bit is set upon assertion of IRESET*, and/or HALT*. It is set whether HALT* is asserted by external sources or by the IM313A. SYSFAIL* is asserted when this bit is set if the SYSFAIL* mask bit (ICR7, bit 7) is cleared.
Bit 7: IRESET* status (read-only). On a VMEbus read, this bit indicates that the IM313A is in a reset state. On a local bus read, this bit is set whenever ACFAIL* is asserted.

Interprocessor Communication Register 7

Name: ICR7
Address: $7F
Description: This register provides semaphores to the five general-purpose interprocessor communication registers (ICR4–0). The remaining bits indicate VMEbus master status, generate HALT* and RESET*, and mask SYSRESET*. The address listed above is the local address.
Bits 4–0: ICR4–0 semaphores. These bits provide semaphores to the five interprocessor communication registers ICR4–0 respectively. Each bit is set when the corresponding ICR is written. These bits must be cleared by the user (i.e., they are not cleared automatically). These bits can be read or written from the local bus or the VMEbus.
Bit 5: VMEbus master status (read-only). This bit is set whenever the IM313A is the VMEbus master, and the IM313A is asserting AS*. This bit is not set when the IM313Ais VMEbus master to an idle bus in ROR and BCAP release modes. Bit 7 of the BESR may be used to indicate that the IM313A is VMEbus master when AS* is not asserted.
Bit 6: HALT* and RESET* control. This bit may be used to assert the HALT* and RESET* pins via software. Whenever this bit is set, the IM313A asserts HALT* and RESET* until this bit is cleared or any reset occurs.
Bit 7: SYSFAIL* mask. When set, the IM313A is prohibited from asserting SYSFAIL* in response to bit 6 of ICR6 being set (which, by default, is set after any reset). This bit must be written after resetting the IM313A to deassert SYSFAIL*.

VMEbus Interrupt Request/Status Register

Name: VIRSR
Address: $83
Description: This register provides status and control of the VMEbus interrupts 7–1.
Bit 0: Register enable/disable. This bit provides enabling and disabling for the remainder of this register.
Bits 7–1: VMEbus interrupt switches. Setting any of these bits asserts the VMEbus IRQi* signals corresponding to the bit positions, if bit 0 is set during the write. These bits are cleared automatically when the interrupt is serviced.

VMEbus Interrupt Vector Base Registers 1–7

Name: VIVBR
Address: $87, $8B, $8F, $93, $97, $9B, $9F For IRQ: 1 2 3 4 5 6 7
Description: Provides the status/ID vector for the VMEbus interrupts.
Bits 7–0: Status/ID Vector. These bits provide the status/ID vector for VMEbus interrupt acknowledge cycles. Address $87 corresponds to IRQ1*. These bits are set to a value of $0F for global and system resets and are unchanged by internal resets.

Transfer Timeout Register

Name: TTR
Address: $A3
Description: Provides control of the local and VMEbus timeout timers.
Bit 0: Include VMEbus acquisition. When set, the local bus timer will include waiting for VMEbus acquisition. When clear, the local bus timer will stop and reset when the VMEbus is requested.
Bit 1: Arbitration timeout. When set, the IM313A as VMEbus arbiter has detected a VMEbus arbitration timeout. This is only used when configured as the VMEbus system controller (SCON* asserted).
Bits 4–2: Local bus timeout period. Defines the local bus timeout.

Bits 4–2	Local Bus Timeout (ms)
000	4 ms
001	16 ms
010	32 ms (default)
011	64 ms
100	128 ms
101	256 ms
110	512 ms
111	Infinite (timer disabled)

Bits 7–5: VMEbus timeout period. Defines the VMEbus timeout.

Bits 7–5	VMEbus Timeout (ms)
000	4 ms
001	16 ms
010	32 ms
011	64 ms (default)
100	128 ms
101	256 ms
110	512 ms
111	Infinite (timer disabled)

Local Bus Timing Register

Name: LBTR
Address: $A7
Description: Provides timing control for PAS* and DS* signals when the IM313A is local bus master. In the following descriptions, n is the binary value specified in the bit fields, and T is one CLK64M clock period. Clock latency may add one additional clock period to these times.
Bits 3–0: Minimum PAS* asserted time. This field specifies the minimum asserted time for the PAS* signal whenever the IM313A is the local bus master. The time is specified by (n + 2)T. The actual asserted time depends on a number of factors including local and VMEbus acknowledge timing.
Bit 4: Minimum DS* deasserted time. This field specifies the minimum deasserted time for the DS* signal whenever the IM313A is the local bus master. A time of 1T is selected when this bit is clear; 2T is selected when this bit is set.
Bits 7–5: Minimum PAS* deasserted time. This field specifies the minimum deasserted time for the PAS* signal whenever the IM313A is the local bus master. The time is specified by (n + 1)T.

Block Transfer Definition Register

Name: BTDR
Address: $AB
Description: Configures master block transfers (both MOVEM and block transfers with local DMA) for boundary crossings, dual-path, and user-defined address modifiers.
Bit 0: Dual-path enable. When set, the IM313A is enabled with the dual-path feature during master block transfers with local DMA. External logic is required when this option is enabled.
Bit 1: AMSR Enable. When set, the IM313A will issue the AM codes based in the address modifier source register for block transfers. This bit effects the AM codes for block transfers only.
Bit 2: When this bit is set, it enables local address 256-byte boundary crossings during DMA block transfer operations. External logic is required to increment latched address lines when this option is enabled.
Bit 3: When this bit is set, it enables VMEbus address 256-byte boundary crossings during DMA block transfer operations. External logic is required to increment latched address lines when this option is enabled.
Bit 7–4: Undefined/Reserved. Bits will be read as 1s.

Interface Configuration Register

Name: ICR
Address: $AF
Description: Controls various features of the IM313A including RMCs, deadlock signaling, metastability delays, and the “turbo” feature.
Bit 0: SCON* value (read-only). Reads the value of the SCON* pin. When set, the IM313A is not the VMEbus system controller. When clear, the IM313A is the VMEbus system controller.
Bit 1: Turbo enable. When set, the IM313A accelerates VMEbus transfers by reducing selected timings by one CLK64M clock period. VMEbus protocols may be violated when the turbo mode is enabled (see section 1.11.5).

Bit 2: Undefined/Reserved.

Bits 4, 3: Deadlock signaling. These bits configure deadlock signaling. Bit 4 is used to enable the assertion of HALT* and LBERR* in addition to the DEDLK* signal in deadlock situations. If bit 4 is enabled, bit 3 may be used to prevent the assertion of HALT* for RMC deadlocks.

Bits 4–3	Deadlock Signaling
0X	DEDLK* only (default)
1X	HALT*, LBERR*, DEDLK*

Note: (HALT* is not asserted for RMC cycles)

Bit 5: RMC control bit 1. When set, the IM313A will request the VMEbus whenever the RMC* is asserted independent of the MWB* signal.

Bit 6: RMC control bit 2. When set, the VMEbus AS* is stretched when RMC* is asserted for VMEbus transfers.

Bit 7: RMC control bit 3. When set, the IM313A qualifies the RMC control bits 5 and 6 with the SIZ1/0 signals. If RMC control bits 5 or 6 are set and the first cycle of the RMC transfer is of byte size, the “set” behaviors are not implemented.

Arbiter/Requester Configuration Register

Name: ARCR
Address: $B3
Description: This register provides configuration of the fairness timeout and DRAM refresh features. The VMEbus request level is also configured from this register.

Bits 3–0: Fairness timer enable. The VMEbus fair requester is enabled in this bit field according to the following table:

Bits 3–0	Timeout Period/Mode
0000	Fairness disabled (default)
1111	Timeout disabled
	All other patterns 2 ms times the number

Bit 4: DRAM refresh. When set, the IM313A will perform CAS-before-RAS (DS* before PAS*) refresh functions.

Bits 6, 5: VMEbus request level. The VMEbus request level is set according to the following table:

Bits 6–5	VMEbus Request Level
00	BR0
01	BR1
10	BR2
11	BR3 (default)

Bit 7: Arbitration mode. When set, the IM313A performs priority VMEbus arbitration. When clear, the IM313A performs round-robin arbitration. This bit is only relevant when the IM313A is configured as the VMEbus system controller (SCON* asserted).

Address Modifier Source Register

Name: AMSR
Address: $B7
Description: This register provides the user-definable address modifiers (AM codes) that can be sourced by the IM313A for VMEbus master cycles, or used in validating AM codes during VMEbus slave cycles.
Bits 5–0: Address modifier code. The AM code that is issued during master cycles or used for qualifying slave cycles. This register is used only when enabled for user-defined AM codes. Otherwise, standard VMEbus AM codes are used.
Bit 6: AM5–3 qualification. When set, the IM313A uses bits 5–3 in qualifying for slave accesses in addition to the address space size information defined by bits 3 and 2 of the SSiCR0s. This bit is overridden if bits 3 and 2 of the SSiCR0s are both set.
Bit 7: AM2–0 generation. When set, the IM313A issues the AM2–0 codes based on the FC2/1 signals. AM5–3 will be issued from bits 5–3 of this register.

Bus Error Status Register

Name: BESR
Address: $BB
Description: This register provides BERR*/LBERR*, self-access, VMEbus mastership, and timeout status. All bits except bit 7 are flags that must be cleared manually by the local processor after being set by status conditions. If these bits are to be used for a specific operation, it is important that they be cleared prior to starting that operation.
Bit 0: Local timeout during VMEbus acquisition. This bit, when set, indicates that a local bus timeout has occurred during an attempted acquisition of the VMEbus.
Bit 1: SLSEL1* self-access. This bit is set when the IM313A is selected by the assertion on the SLSEL1* signal, while operating as VMEbus mas-ter.
Bit 2: SLSEL0* self-access. This bit is set when the IM313A is selected by the assertion on the SLSEL0* signal, while operating as VMEbus master.
Bit 3: Local bus timeout. This bit, when set, indicates a local bus timeout occurred without qualification.
Bit 4: VMEbus timeout. This bit, when set, indicates the IM313A has signaled a VMEbus timeout. This bit is relevant only if the IM313A is system controller and the VMEbus timeout is enabled.
Bit 5: VMEbus bus error. This bit is set when a VMEbus bus error is signaled (BERR* asserted).
Bit 6: Local bus error. This bit is set when a local bus error is signaled by a source other then the IM313A (LBERR* asserted to the IM313A).
Bit 7: VMEbus mastership. This bit is set whenever the IM313A is VMEbus master.

DMA Status Register

Name: DMASR
Address: $BF
Description: This register provides status of a IM313A DMA transfer. This includes the block transfer with local DMA function. Status bits are included to show various BERR* and LBERR* statuses and DMA termination statuses.
Bit 0: Block transfer in progress. This bit, when set, indicates an interleaved block transfer is in progress. Once set, this bit is cleared automatically by the IM313A after completion of the local DMA operation, or by resetting the IM313A.

Bit 1: LBERR* during DMA transfer. This bit, when set, indicates a LBERR* was signaled during a DMA transfer. Once set, this bit must be cleared manually by writing a 0 (zero) to this bit location, or by resetting the IM313A.

Bit 2: BERR* during DMA transfer. This bit, when set, indicates a BERR* was signaled during a DMA transfer. Once set, this bit must be cleared manually by writing a 0 (zero) to this bit location, or by resetting the IM313A.

Bit 3: Local bus error (read-only). This bit is set when a local bus error is signaled by a source other then the IM313A (LBERR* asserted to the IM313A). This bit is a read-only copy of bit 6 of the BESR.

Bit 4: VMEbus bus error. This bit is set when a VMEbus bus error is signaled (BERR* asserted). This bit is a copy of bit 5 of the BESR.

Bits 5, 6: Undefined/Reserved. These bits will be read as 1s.

Bit 7: Master write post information stored. This bit is set whenever master write post information is stored.

Slave Select 0 Control Register 0

Name: SS0CR0

Address: C3

Description: This register provides control of the slave selection 0 facilities of the IM313A. Enabling of the LIRQ2* timer interrupt is also configured in this register.

Bits 1–0: Local transfer mode. These bits set the local transfer mode when the IM313Ais local bus master for both slave and master block transfers.

Bits 1–0	Mode
00	No support is given for slave block transfers on SLSEL0*. The IM313Awill BERR* any attempt to receive a VMEbus block transfer. Master block transfers with local DMA will not function in this mode.
01	Emulate single-cycle transfers on the local bus. In this mode, the IM313Aemulates single-cycle transfers when performing slave block transfers and master block transfers with local DMA. By emulating single-cycle transfers, the IM313A toggles the PAS* for each cycle. DSACKi must toggle for each transfer and not be held asserted.
10	Accelerated transfers on the local bus. In this mode, the IM313A asserts the PAS* signal for the entire slave block transfer and master block transfer with local DMA. The DSACKi* signals should be held asserted in this mode.
11	Undefined/Reserved.

Bits 3–2: Address space configuration. The SLSEL0* address space is configured according to the following table:

Bits 3–2	Address Space
00	A32 (extended) (default)
01	A24 (standard)
10	A16 (short)
11	User defined, uses AMSR

Bit 4: D32 enable. D32 slave operations are enabled for SLSEL0* when this bit is set. This bit has no effect for enabling D32 master accesses. This bit also controls byte-lane switching for D16 Block transfers. When set ISOBE* and SWDEN* alternate states thus alternating which D16 bus data is placed. When clear, only SWDEN* is asserted for D16 block transfers.

Bit 5: Supervisory access. When set, SLSEL0* slave accesses are restricted to supervisory accesses. Other accesses are BERRed. Supervisory accesses are checked with the AM(2) signal.

Bits 7–6: Periodic interrupt timer enable. These bits enable and determine the frequency of the periodic LIRQ2* interrupt. If the IM313Ais to handle this local interrupt, LICR2 must be enabled. The frequencies for this interrupt are given below:

Bits 7–6	Timer Mode
00	Timer disabled (default)
01	50-Hz output on LIRQ2*
10	1000-Hz output on LIRQ2*
11	100-Hz output on LIRQ2*

Slave Select 0 Control Register 1

Name: SS0CR1
Address: $C7
Description: This register provides the various access and acquisition timings for slave transfers and slave block transfers for SLSEL0* in addition to data acquisition timing for master block transfers with local DMA.
Bits 3–0: Timing field 0. This bit field establishes the following data access/acquisition timings:

- single-cycle slave access timing for SLSEL0* (SAT)
- first cycle of a slave block transfer for SLSEL0* (SBAT0)
- first cycle of a master block transfer with local DMA (MBAT0)

The delays are programmed in multiples of the CLK64M clock period according to the following table:

Bits 3–0	CLK64M Clock Period Delay
0000	3
0001	4
0010	4
0011	5
0100	5
0101	6
0110	6
0111	7
1000	7
1001	8
1010	8
1011	9
1100	9
1101	10
1110	10
1111	11

Note: The major differences between VIC068A and IM313 are given in blue

Bits 7–4: Timing Field 1. This bit field establishes the following data access/acquisition timings:

- second and subsequent cycle of a slave block transfer for SLSEL0*(SBAT1)
- second and subsequent cycle of a master block transfer with local DMA (MBAT1)

The delays are programmed in multiples of the CLK64M clock period according to the following table:

Bits 7–4	CLK64M Clock Period Delay
0000	3
0001	4
0010	4
0011	5
0100	5
0101	6
0110	6
0111	7
1000	7
1001	8
1010	8
1011	9
1100	9
1101	10
1110	10
1111	11

Note: The major differences between VIC068A and IM313 are given in blue

Slave Select 1 Control Register 0

Name: SS1CR0
Address: $CB
Description: This register provides control of the slave selection 1 facilities of the IM313A. Master and slave write posting is enabled in this register as well.
Bits 1–0: Local Transfer Mode. These bits set the local transfer mode when the IM313Ais local bus master for both slave and master block transfers.

Bits 1–0	Mode
00	No support is given for slave block transfers on SLSEL1*. The IM313A will BERR* any attempt to receive a VMEbus block transfer.
01	Emulate single-cycle transfers on the local bus. In this mode, the IM313A emulates single-cycle transfers when performing slave block transfers. By emulating single-cycle transfers, the IM313A toggles PAS* for each cycle. DSACKi* must toggle for each transfer and not be held asserted.
10	Accelerate transfers on the local bus. In this mode, the IM313A asserts PAS* for the entire slave block transfer. The DSACKi* signals should be held asserted in this mode.
11	Undefined/Reserved.

Bits 3–2: Address Space Configuration. The SLSEL1* address space is configured according to the following table:

Bits 3–2	Address Space
00	A32 (extended) (default)
01	A24 (standard)
10	A16 (short)
11	User defined, uses AMSR

Bit 4: D32 enable. D32 slave operations are enabled for SLSEL1* when this bit is set. This bit has no effect for enabling D32 master accesses.
Bit 5: Supervisory access. When set, SLSEL1* slave accesses are restricted to supervisory accesses. Other accesses are BERR ed. Supervisory accesses are checked with the AM(2) signal.
Bit 6: Master write post enable. When set, master write posting is enabled.
Bit 7: Slave write post enable. When set, slave write posting is enabled.

Slave Select 1 Control Register 1

Name: SS1CR1
Address: $CF
Description: This register provides the various access and acquisition timings for slave transfers and slave block transfers for SLSEL1*.
Bits 3–0: Timing field 0. This bit field establishes the following data access/acquisition timings:
• single-cycle slave access timing for SLSEL1* (SAT)
• first cycle of a slave block transfer for SLSEL1* (SBAT0)

The delays are programmed in multiples of the CLK64M clock period according to the following table:

Bits 3–0	CLK64M Clock Period Delay
0000	3
0001	4
0010	4
0011	5
0100	5
0101	6
0110	6
0111	7
1000	7
1001	8
1010	8
1011	9
1100	9
1101	10
1110	10
1111	11

Note: The major differences between VIC068A and IM313 are given in blue

Bits 7–4: Timing field 1. This bit field establishes the following data access/acquisition timing:
• second and subsequent cycle of a slave block transfer for SLSEL1*(SBAT1)

The delays are programmed in multiples of the CLK64M clock period according to the following tables:

Bits 7–4	CLK64M Clock Period Delay
0000	3
0001	4
0010	4
0011	5
0100	5
0101	6
0110	6
0111	7
1000	7
1001	8
1010	8
1011	9
1100	9
1101	10
1110	10
1111	11

Note: The major differences between VIC068A and IM313 are given in blue

Release Control Register

Name: RCR
Address: $D3
Description: This register configures the VMEbus release mode. The burst count for block transfers with local DMA is also configured in the RCR.
Bits 5-0: Block transfer burst length. The burst length for both MOVEM block transfers and block transfers with local DMA are configured in this bit field. The value indicates the number of cycles per block transfer (not the number of bytes). A value of 0 in this bit field indicates the maximum 64 cycles per burst. All other values correspond directly to the burst count.
Bits 7-6: Release mode. This bit field defines the release mode used by the IM313A when releasing the VMEbus after the completion of a VMEbus transfer.

Bits 7–6	Release Mode
00	ROR—Release on Request (default)
01	RWD—Release When Done
10	ROC—Release on BCLR* assertion
11	BCAP—VMEbus Capture and Hold

Block Transfer Control Register

Name: BTCR
Address: $D7

Description: The BTCR provides control of the IM313A block transfers. The local interleave periods and data direction are defined in this register. The enabling bits for all of the VIC068A's block transfer modes are located here as well. These enabling bits are mutually exclusive and more than one should not be set at the same time.

Bits 3–0: Interleave period.The interleave period for block transfers is defined here. The interleave period is 250 ns times the value programmed in this bit field.
Bit 4: Data direction. This bit defines the direction of a block transfer with local DMA (MOVEM data direction determined by the R/W* signal). When set, VMEbus block reads occur. When clear, VMEbus block writes occur.
Bit 5: MOVEM enable. When set, MOVEM transfers are enabled. After this bit is set, the next VMEbus transfer is treated as the start of a VMEbus block transfer. Clearing this bit concludes a MOVEM block transfer in progress. It is important to set this bit immediately before and clear this bit immediately after the actual MOVEM transfer.
Bit 6: Block transfer with local DMA enable. When set, block transfers with local DMA are enabled. After this bit is set, the next assertion of MWB* is considered the initiation cycle of a VMEbus block transfer with local DMA. It is important to set this bit immediately before and clear this bit immediately after the actual block transfer.
Bit 7: Special purpose. For normal operation set this bit to 0.

Block Transfer Length Registers 1–0

Name: BTLR1–0
Addresses: $DB (BTLR1), $DF (BTLR0)

Description: These registers configure the byte count for block transfers with local DMA. BTLR1 is considered the most significant byte and BTLR0 the least significant. Bit 0 of BTLR0 must never be set because this implies at least one 8-bit transfer is required to complete the block transfer. Only D16 and D32 block transfers are supported. If bit 0 of BTLR0 is set, the block transfer length is ignored and only one burst is performed.
Bits 7–0: Block transfer length. Defines the block transfer length in bytes. BTLR1 contains the most significant 8 bits of the length, and BTLR0 the least.

System Reset Register

Name: SRR
Address: $E3

Description: The system reset register provides the means to perform a VMEbus system reset (SYSRESET* asserted). Writing a value of $F0 causes this function to occur. A system reset is also performed within the IM313A.
Bits 7–0: System reset field. Writing this bit field with a value of $F0 causes SYSRESET* to be asserted for a minimum of 200 ms and a system reset to be performed within the VIC068A.

Interrupts

VMEbus and local bus interrupts are generated and handled by IM313A.

- **VMEbus Interrupter**

Registers used for interrupts generation:

- VMEbus Interrupt Request/Status Register (VIRSR), address 83
- VMEbus Interrupt Vector Base Registers 1-7 (VIVBR1-7), address 87-9F

The VIRSR control the assertion of VMEbus interrupts. Once the IM313A recognizes a valid interrupt acknowledge it places the status/ID vector located in VIVBR1-7 registers on D(7-0) bus.

- **VMEbus and local Interrupt Handler**

Registers used for interrupts handling:

- VMEbus Interrupter Interrupt Control Registers (VIICR), address 03
- VMEbus Interrupt Control Registers 1-7 (VICR1-7), address 07-1F
- DMA status Interrupt Control Register (DMASICR), address 23
- Local Interrupt Control Registers 1-7 (LICR1-7), address 27-3F
- ICGS Interrupt Control Register (ICGSICR), address 43
- ICMS Interrupt Control Register (ICMSICR), address 47
- Error Group Interrupt Control Register (EGICR), address 4B
- ICGS Interrupt Vector Base Register (ICGSIVBR), address 4F
- ICMS Interrupt Vector Base Register (ICMSIVBR), address 53
- Local Interrupt Vector Base Registers (LIVBR), address 57
- Error Group Interrupt Vector Base Registers (ECIVBR), address 5B

The IM313A can be configured to handle VMEbus interrupt and/or local bus interrupt.

For VMEbus interrupt, if VICR1-7(bit 7) is clear, the IM313A handles all pending interrupts on that respective level. Only one device on a VMEbus system can be configured as interrupt handler.

For local bus interrupt, if LICR1-7(bit 7) is clear, the IM313A handles the corresponding local interrupt.

Block transfer functions

- **Master block transfer**

Two type of master block transfer exist:

- MOVEM : IM313A is slave for local bus and master for VMEbus.
- VMEbus Block transfer with local bus DMA : IM313A is master for local bus and VMEbus

Registers used in master block transfer functions:

- Block Transfer Control Register (BTCR), address D7
- Block Transfer Definition Register (BTDR), address AB
- Release Control Register (RCR), address D3
- Block Transfer Length Registers (BTLRs), address DB and DF
- Local Bus Timing Register (LBTR), address A7
- Slave Select 0 Control Register 1 (SS0CR1), address C7
- DMA status Register (DMASR), address BF
- DMA status Interrupt Control Register (DMASICR), address 23
- Address Modifier Source Register (AMSR), address B7

For master block transfer AM code output are generated by using the table 1-6 if BTDR register bit 1 is low, AM is equal to AMSR register if BTDR register bit 1 is high.

- **MOVEM block transfer**

MOVEM operations cause **multiple single cycle** masters' operations on the LocalBus to be formatted as **Block transfer** operation on VMEbus, as the AS* output signal is driven and kept low until the burst is completed.

The only advantage of this mode is that all VME accesses put out block transfer **AM codes** on the VME side of the bus. Also, VIC068's counters are not active, so **no boundary crossing** detection takes place.

- **VMEbus Block transfer with local bus DMA**

The block transfer with local DMA is block transfer in which the IM313A becomes not only the VME bus master but the local bus master as well. For this type of transfer the IM313A contains two 8-bit address counters that can automatically increment the address for both the local (CPU) side and the VME bus side.

The steps for this block transfer are:

- Register initialization : BTLR0 ($DB), BTLR1 ($DF), BTDR ($AB), LBTR ($A7), BTCR($D7), RCR ($D3)
- Pseudo-write cycle :
    - Wait MWB* after BTCR(6) setting
    - Put LA(7:0) in VMEbus address counter and LD(7:0) in Local DMA address counter. Then, assert LADO and BLT* to latch remainder of LA[+:8] and LD[+:8] as VMEbus address and local bus address
    - Assert DSACKi* to terminate the cycle

- Request VMEbus
- When VMEbus is granted, request local bus (send LBR*)
- When local bus is granted, put the local DMA address counter on the local address bus.
- Then, it accesses the local data by asserting local address and data strobes
-

<u>256 byte address boundary crossing on VMEbus :</u>

It is not allowed by the VMEbus specification but if IM313A is configured for VME boundary crossing (BTDR register bit 3) it deassert AS* without release bus (BBSY* is held asserted). It enables to not lose the mastership for IM313A during the boundary crossing.

<u>256 byte address boundary crossing on local bus :</u>

The local boundary crossing is enabling in BTDR (bit 2). In this case, BLT* toggle before the boundary crossing to enable external counters to be incremented.

Interleave period and dual-path option :

During interleave period (time between burst) slave cycles can be performed. Master cycles are allowed only if "Dual-path" mode is programmed in BTDR register (bit 0).

- **Slave block transfer**

Register used for this function:

- Local Bus Timing Register (LBTR), address A7
- Slave Select 0 Control Register 0 (SS0CR0), address C3
- Slave Select 1 Control Register 0 (SS1CR0), address CB

There are three blocks transfer mode, programmed in SS0CR0 (bit 1-0) if block transfer activated by SLSEL0* and SS1CR0 (bit 1-0) if block transfer activated by SLSEL1*.

- No block transfer
- Support block transfer and emulate single-cycle (PAS* and DSACKi* toggle for each transfer)
- Support block transfer in DMA mode (PAS* and DSACKi* not toggled)

Miscellaneous features

There are additional features of IM313A

Reset

There is an internal power-On-reset.

Additionally, there are three external sources of reset. The priority is as following

- Global reset
- Internal reset
- System reset

The global reset is initiated by asserting IPL0 after IRESET is asserted. It resets the entire device.

The internal reset is initiated by asserting IRESET*. It resets internal circuitry and selected register.

The system reset is VMEbus defined reset. It resets internal circuitry and selected register. The device can receive or generate a system reset. If it generates a system reset, it resets itself. There are two ways to generate a system reset:

- Write "F0" in SRCR register
- Implement internal or global reset while configured as VMEbus system controller

Local bus timeout timer
Dram refresh controller
Rescinding outputs
Turbo mode

External Buffer control

For each type of operations, IM313A drive 12 buffer control output. They control the latching and enabling of external data and address.

Some modifications on the external buffer control timing are implemented.

The buffer control signals are used as buffer enable, latch enable and direction control for the VME, intermediate and local data and address busses.

In each functional cycles, address and data busses have to be transferred either from local to VME side, or vice versa.

One of the reasons for modifications is that in some transfer cycles buffers are enabled to transfer data too early, i.e. the data to be transferred is in high-impedance state when the corresponding buffer enable signal is activated. This might cause a lot of glitches and noise on the power supply lines.

Another reason for modifications is connected with power supply noise. Such noise may appear if there is simultaneous switching of great number of address and/or data bus lines.

All modifications were done according to the following rules:

1. Buffers must be enabled to transfer data only when the corresponding data is stable.
2. There must not be more than 16 simultaneously changing data and/or address bits, caused by one and the same clock edge driven from VIC068.
3. The external buffer control signals modifications must not change the global cycle duration

.
Here below is a list of the functions, utilized by the system, and requiring a modification in the external buffer control signal:

Master read
Master write
Master RMC (read modify cycle)
Slave read
Slave write
Slave TAS
Interrupt cycles – ICMS, VME and local
Register access

Electrical features

Parameter	Symbol	Min	Max	Units	Comment
Power supply	VCC	4.5	5.5	V	I/O
Operating temperature		-40	+85	°C	
Storage temperature		-50	+125	°C	

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power supply	VDD	-0.3	7	V
Input voltage	Vin	-0.3	VDD+0.3	V
Output voltage	Vout	-0.3	VDD+0.3	V

Digital pins Characteristics

Pins AS, DS1, DS0, BCLR, SYSCLK (64mA)

Parameter	Symbol	Test Condition	Min	Max	Unit
Low level input voltage	V_{IIL}			0.8	V
High level input voltage	V_{IIH}		2		V
Low level output voltage	V_{OL}	VCC = Min IOL = 48mA, 56mA, 64mA		0.6	V
High level output voltage (source current : 4 mA)	V_{OH}	VCC = Min IOH = -3 mA	2.4		V
Maximum Input Leakage Current	Il	VCC=Max VIN = 0.6-2.4		±5	µA

Pins Low Drive (8mA)

Parameter	Symbol	Test Condition	Min	Max	Unit
Low level input voltage	V_{IIL}			0.8	V
High level input voltage	V_{IIH}		2		V
Low level output voltage	V_{OL}	VCC = Min IOL =8mA		0.6	V
High level output voltage (source current : 4 mA)	V_{OH}	VCC = Min IOH = -8 mA	2.4		V
Maximum Input Leakage Current	Il	VCC=Max VIN = 0.6-2.4		±5	µA

Pins MediumDrive (48mA)

Parameter	Symbol	Test Condition	Min	Max	Unit
Low level input voltage	V_{IIL}			0.8	V
High level input voltage	V_{IIH}		2		V
Low level output voltage	V_{OL}	VCC = Min IOL =48mA		0.6	V
High level output voltage (source current : 4 mA)	V_{OH}	VCC = Min IOH = -3 mA	2.4		V
Maximum Input Leakage Current	Il	VCC=Max VIN = 0.6-2.4		±5	µA

Thermal behavior

Temperature range: industrial, -40°C to 85°C

Maximum junction temperature for the technology used is 150°C

Thermal resistance between junction and ambient air is 65°C/W for MQFP160 package.

Calculation of power consumption: there are two configurations:

- Nominal power: peripherals 400mW, core 100 mW, total 500 mW. This corresponds to an average activity of the component.
- Peak power: peripherals 700 mW, core 150 mW, total 850 mW. This corresponds to a maximum activity of the core and all outputs drive maximum current.

With this formula: $Tj=Ta + \theta j\text{-}a \times P$, where Tj = junction temperature, Ta = ambient temperature, $\theta j\text{-}a$ Thermal resistance between a junction and ambient air, P: Power consumption, we can calculate the maximum chip junction temperature:

Tj = 85°C + 65°Cx0,850 = 140 °C for MQFP160 package.

Thermal resistance between junction and ambient air is 25°C/W for Ceramic package (PGA or QFP).

Tj = 85°C + 25°Cx0,850 = 106 °C for Ceramic package (PGA or QFP).

Ordering information

Pakage Type	Temperature	Order number
Ceramic PGA 144	-40°C to +85°C	IM313A FPC
Ceramic PGA144	-55°C to +85°C	IM313A CPC
Ceramic PGA144	-55°C to +85°C MIL_STD_883 class level B	IM313A CPC/883B
Plastic PQFP160 (ROHS compliant)	-0°C to +70°C	IM313A BHL/160
Plastic PQFP160 (ROHS compliant)	-40°C to +85°C	IM313A FHL/160
Plastic TQFP144 (RoHS compliant)	0°C to +70°C	IM313A BHL/144
Plastic TQFP144 (RoHS compliant)	-40°C to +85°C	IM313A FHL/144
Ceramic CQFP160	-40°C to +85°C	IM313A FHC
Ceramic CQFP160	-55°C to +125°C	IM313A CHC
Ceramic CQFP160	-55°C to +125°C MIL_STD_883 class level B	IM313A CHC/883B

For military temperature range (-55°C, 125°C) products in PGA or CQFP packages, please contact ID MOS.

Contacts

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Annexe : AC Performance Specifications

The major differences between VIC068A and IM313 are given in blue. These differences are in the logic for the signal assertion. There are additional timing drawings for these differences.

The timings are given for Industrial conditions

Arbitration				
	Operation	Note	Im313 (max)	VIC Spec (max)
A1	BRi[0] : BBSY[H]		2.5T+5	3T+26
A2	BRi[0] : BBSY[L]		3.5T+16	3.5T+34
A3	BRi[0] : BGiOUT[L]		4T	4T+26
A4	BRi[0] : BCLR[L]		3	16
A5	BGiIN[0] : BGiOUT[L]		16	18
A6	BGiIN[0] : BBSY[L]		32	24
A7	BGiIN[0] : BRi [H]		3T+31	3T+27
A8	BGiIN[1] : BGiOUT[H]		16	21
A9	BBSY[0] : BGiOUT[H]		3	22
A10	BBSY[1] : BGiOUT[L]		4T+32	4T+26
A11	BBSY[1] : BCLR[L]		3	2T+25

Master Access				
	Operation		Im313 (max)	VIC Spec (max)
B1	BGiIN[0] : DENO[L]	write	2T+8	3T+37
B2	BGiIN[0] : LADO[H]	Not existing		
B3	BGiIN[0] : AS[L]		5T+6	6T+29
B4	BGiIN[0] : A[7:1] valid		2T+4	3T+32
B5	BGiIN[0] : LWORD[H/L]		2T+4	3T+32
B6	BGiIN[0] : WRITE[H/L]		2T+4	3T+32
B7	BGiIN[0] : ABEN[L]		2T+4	3T+36
B8	PAS[0] & MWB[0] : BRi[L]		8	22
B9	PAS[0] & MWB[0] : ISOBE[L]	write	7	23
B9a	DTACK : ISOBE[L]	read	7 + 2T	
B10	PAS[0] & MWB[0] : LADO[H]	Not existing		
B11	PAS[0] & MWB[0] : BBSY[L]	Not existing		
B12	PAS[0] & MWB[0] : ABEN[L]		2T+3	2.5T+37
B13	PAS[0] & MWB[0] : A[7:1]		2T+3	2.5T+37
B14	PAS[0] & MWB[0] : LWORD[H/L]		2T+3	2.5T+37
B15	PAS[0] & MWB[0] : WRITE[H/L]		2T+3	2.5T+37
B16	PAS[0] & MWB[0] & DS[0] : DS1/0[L]		5.5T+14	5.5T+47
B17	PAS[0] & MWB[0] : SWDEN[L]	write	7	12
B17a	DTACK : SWDEN[L]	read	7 + 1.5T	
B18	DTACK : DENIN[L]	read	7 + 1T	
B19	DTACK : DENIN1[L]	read	7	
B20	PAS[0] & MWB[0] & DS[0] : AS [L]		6T+6	5.5T+29

B21	R/W [0] : DDIR [H]	Write	3	23
B22	R/W [1] : DDIR [L]	Write	3	14
B23	D[7:0] : LD[7:0]	Read	15	18
B24	DTACK[0] : LEDI[H]	Read	4T + 4	4T+29
B25	DTACK[0] : DSACKi[L]		3T	31
B26	PAS[1]&DS[1] : DSACKi[H]		6	20
B27	PAS[1] : AS[H]		3	31
B28	DS[1] : ISOBE[H]		10	24
B29	DS[1] : SWDEN[H]		9	10
B30	DS[1] : DENIN1[H]	Read	4	20
B31	DS[1] : DENIN[H]	Read	4	20
B32	DS[1] : LD[7:0] Invalid	Read	9	22
B33	DS[1] : LD[7:0] Hi-Z	Read	9	22
B34	DS[0] : DSACKi[L]	Write Post	T+51	T+32
B35	DS[0] : LADO[H]	Write Post	50	39
B36	DS[0] : LEDO[H]	Write Post	T+34	T+18

VIC as Local Bus Master				
	Operation		Im313 (max)	VIC Spec (max)
C1	LBG[0] : PAS[L]		6T+33	6T+33
C2	LBG[0] : LA[7:0] valid		4T+21	4T+37
C3	LBG[0] : SIZ[1:0] valid		2T+3	2T+21
C4	LBG[0] : FC [2:1] valid		2T+3	2T+21
C5	LBG[0] : LD[7:0] driven	Write	4T+21	4T+39
C6	LBG[0] : LAEN[H]		4T+20	4T+44
C7	LBG[0] : ISOBE[L]		4T+23	4T+39
C8	LBG[0] : SWDEN[L]		4T+23	4T+41
C9	LBG[0] : DDIR[H]	Write	4T+21	4T+39
C10	LBG[0] : DENIN1[L]	Write	4T+21	4T+38
C11	LBG[0] : DENIN[L]	Write	4T+21	4T+35
C12	LBG[0] & DS1/0[0] & WRITE[0] :R/W[L]	Write	4T+21	4T+40
C13	LBG[0] & DS1/0[0] : DS[L]		6T+34	6T+42
C14	PAS[0] : DS[L]		1	15
C15	LBR[H] : LBG[1]	NA, External timing		

Slave Access				
	Operation		Im313 (max)	VIC Spec (max)
D1	SLSELi[0] & AS[0] : LBR[L]		45	36
D2	SLSELi[0] & AS[0] & DS1/0[1] : LADI[H]		40	26
D3	LD[7:0] : D[7:0]	Read	15	16
D4	DSACKi[0] : LEDO[H]	read	SAT+0.5T+25	SAT+0.5T+36
D4a	DSACKi[0] : ISOBE[L], SWEDEN[L]	read	7	
D4b	DSACKi[0] : DENO[L]	read	7 + 1T	
D5	DSACKi[0] : DTACK[L]		SAT+0.5T+42	SAT+0.5T+47
D6	DS1/0[0] : DTACK[L]	Write post	2T+15	3.5T+29
D7	DS1/0[0] : LEDI[H]	Write post	30	43
D8	AS[1] : LA[7:0], R/W invalid		6	42
D9	AS[1] : LA[7:0], R/W high Z		6	42
D10	AS[1] : FC[2:1] invalid		35	44
D11	AS[1] & DSACKi[1] : FC[2:1] high Z		35	44
D12	AS[1] : SIZ[1:0] invalid		35	34
D13	AS[1] & DSACKi[1] : SIZ[1:0] high Z		1T+19	1T+19
D14	AS[1] : ISOBE[H]		7	31
D15	AS[1] : SWDEN[H]		6	25
D16	AS[1] : DENIN1[H]	write	5	28
D17	AS[1] : DENIN[H]	write	5	28
D17a	AS[1] : LEDI[L]	write	5 + 1T	
D18	AS[1] & DSACKi[1] : LBR[H]		62	27

D19	AS[1] : LAEN[L]		50	43
D20	DS1/0[1] : LD[7:0], invalid	write	5	30
D21	DS1/0[1] : LD[7:0], high Z	write	5	30
D22	DSACKi[0] : PAS[H]		SAT+0.5T+24	SAT+0.5T+46
D23	DSACKi[0] : DS[H]		SAT+0.5T+24	SAT+0.5T+41
D24	DS1/0[1] : DTACK[H]		33	28

Interrupt				
	Operation		Im313 (max)	VIC Spec (max)
E1	IACKIN[0] : IACKOUT[L]		4	17
E2	IACKIN[1] : IACKOUT[H]		4	19
E3	FCIACK[0] & PAS[0] : BRi[L]		6T+39	6T+42
E4	FCIACK[0] & PAS[0] : IACK[L]		11.5T+30	8.5T+3
E5	FCIACK[0] & PAS[0] : LD[7:0] driven		6T+34	6T+52
E6	FCIACK[0] & PAS[0] : LD[7:0] valid		9T+2	10T+33
E7	FCIACK[0] & PAS[0] : LIACKO[L]		6T+32	6T+33
E8	IRQi[0] : IPL		17	34
E9	BGiIN[0] : BBSY[L]		32	33
E10	BGiIN[0] : AS[L]		4T+6	4T+28
E11	BGiIN[0] : DS1/0[L]		4T+6	4T+46
E12	BGiIN[0] : IACK[L]		7	40
E13	PAS[0] : ISOBE[L]		6T+49	6T+40
E14	PAS[0] : SWDEN[L]		6T+41	6T+38

E13a	DTACKn[0] : ISOBE[L]		4 + 1.5T	
E14a	DTACKn[0] : SWDEN[L]		4 + 1T	
E15	IPLi : IPLi (skew)		3	12
E16	DTACKn[0] : DENIN1[L]		4	

Master block transfer with local DMA (Initiation cycle)				
	Operation		Im313 (max)	VIC Spec (max)
F1	MWB[0] & PAS[0] & DS[0] : BRi[L]		3T+32	2T+33
F2	BGiIN[0] : LBR[L]		4T	5T+44
F3	MWB[0] & PAS[0] & DS[0] : LBR[L]		10T	6T+44
F4	MWB[0] & PAS[0] & DS[0] : LADO[H]		2T+19	2T+36
F5	MWB[0] & PAS[0] & DS[0] : BLT[L]		2T	2T+29

Master block transfer with local DMA (Write)				
** First cycle **				
	Operation		Im313 (max)	VIC Spec (max)
G1	DSACK[0] & DS[L] : DS[H]		MBAT0 +1.5T+8	MBAT0+0.5T+43
G2	DSACK[0] & DS[L] : LEDO[H]		MBAT0+16	MBAT0+0.5T+37
G3	DSACK[0] & DS[L] : LA[7:0] valid		MBAT0+ 1.5T+24	MBAT0+1.5T+36
G4	DSACK[0] & DS[L] : DSi[L]		MBAT0+ 3.5T+39	MBAT0+3.5T+39
G5	DTACK[0]: LEDO[L]		48	33
G6	DTACK[0]: DSi[H]		46	51
G7	DTACK[0]: A[7:0] valid		48	48

G8	DS[H]: DS[L]		DST + 4	DST+1.5T-14
** Second cycle **				
G9	DSACK[0] & DS[L] : DS[H]		MBAT1+3T +42	MBAT1+0.5T+43
G10	DSACK[0] & DS[L] : LEDO[H]		MBAT1+3T +39	MBAT1+0.5T+37
G11	DSACK[0] & DS[L] : LA[7:0] valid		MBAT1+4T +20	MBAT0+1.5T+36
G12	DSACK[0] & DS[L] : DSi[L]		MBAT1+5T +74	MBAT1+3.5T+30
G13	DTACK[0]: LEDO[L]		48	33
G14	DTACK[0]: DSi[H]		46	46
G15	DTACK[0]: A[7:0] valid		50	48
G16	DTACK[0]: DS[H]		1.5T+40	1.5T+46
G17	LEDO[L] : LEDO[H]		1T+3	1.5T+26

Master block transfer with local DMA (Read)				
** First cycle **				
	Operation		Im313 (max)	VIC Spec (max)
H1	DTACK[0]: LEDI[H]		3T	3T+25
H2	DTACK[0]: DSi[H]		2T+14	3T+30
H3	DTACK[0]: A[7:0] valid		2.5T+10	2.5T+45
H4	DTACK[0]: DS[L]		2.5T+10	2.5T+40
H5	DSACK[0] & DS[L] : DS[H]		MBAT0+0.5T+18	MBAT0+0.5T+40
H6	DSACK[0] & DS[L] : LEDI[L]		MBAT0+ 0.5T+ 33	MBAT0+0.5T+50
H7	DSACK[0] & DS[L] : LA[7:0] valid		MBAT0+1.5T+19	MBAT0+1.5T+32
H8	DSACK[0] & DS[L] : DSi[L]		MBAT0+42	MBAT0+0.5T+76
** Second cycle **				

H9	DTACK[0]: LEDI[H]		3T	3T+25
H10	DTACK[0]: DSi[H]		2T+14	3T+30
H11	DTACK[0]: A[7:0] valid		48	45
H12	DTACK[0]: DS[L]		34	40
H13	DSACK[0] & DS[L] : DS[H]		MBAT1+30	MBAT1+0.5T+38
H14	DSACK[0] & DS[L] : LEDI[L]		MBAT1+46	MBAT1+0.5T+46
H15	DSACK[0] & DS[L] : LA[7:0] valid		MBAT1+1.5T+22	MBAT1+1.5T+33
H16	DSACK[0] & DS[L] : DSi[L]		MBAT1+0.5T+38	MBAT1+0.5T+76

Master block transfer with local DMA (Read)				
	Operation		Im313 (max)	VIC Spec (max)
J1	DS[L]: BLT[H]		22	32
J2	DS[H]: BLT[L]		18	19
J3	DSi[L]: LADO[H/L]		11	23
J4	DSi[H]: LADO[L/H]		3	18

Slave block transfer (Write)				
** First cycle ** - see C1, C2, etc				
** Second cycle **				
	Operation		Im313 (max)	VIC Spec (max)
K1	DSi[0]: LEDI[H]		32	22
K2	DSi[0]: DS[L]		50	36
K3	DSACK[0] & DS[L] : DS[H]		SBAT+0.5T+24	SBAT+0.5T+42
K4	DSACK[0] & DS[L] : DTACK[L]		SBAT+0.5T+13	SBAT+0.5T+53

K5	DSACK[0] & DS[L] : ISOBE[H]			SBAT+0.5T+56
K6	DSACK[0] & DS[L] : SWDEN[H]			SBAT+0.5T+52
K7	DSACK[0] & DS[L] : LA[7:0] valid		SBAT+1.5T+23	SBAT+1.5T+36
K8	DSACK[0] & DS[L] : LEDI[L]		SBAT+0.5T+87	SBAT+0.5T+48
K9	DSi[1]: DTACK[H]		33	28

Slave block transfer (Read)				
** First cycle ** - see C1, C2, etc				
** Second cycle **				
	Operation		Im313 (max)	VIC Spec (max)
L1	DSi[1]: LEDO[L]		48	24
L2	DS[H]: DS[L]		DST+2	DST+1.5T-3
L3	DSi[0]: DENO[L]		4	22
L4	DSACK[0] & DS[L] : LEDO[H]		SBAT+0.5T +9	SBAT+0.5T+37
L5	DSACK[0] & DS[L] : DS[H]		SBAT+0.5T +24	SBAT+0.5T+43
L6	DSACK[0] & DS[L] : DTACK[L]		SBAT+0.5T +10	SBAT+0.5T+48
L7	DSACK[0] & DS[L] : LA[7:0] valid		SBAT+1.5T +23	SBAT+1.5T+36
L8	DSi[1]: DENO[H]		4	20
L9	DSi[1]: DTACK[H]		33	21
L10	LEDO[L]]: LEDO[H]		T+2	1.5T+26
L11	DTACK [0]: DS[H]		1T	1.5T+46

Register Access				
	Operation		Im313 (max)	VIC Spec (max)
M1	PAS[0] & DS[0] & CS[0] : DSACK[L]	write	5T+3	5T+35
M1a	PAS[0] & DS[0] & CS[0] : DSACK[L]	read	5T+27	5T+35
M2	PAS[0] & DS[0] & CS[0] : LD[7:0] valid		4T+2	4T+29
M3	AS[0] & ICFSEL[0] : DTACK[L]		4T+12	4T+31
M4	PAS[0] & DS[0] & CS[0] : ISOBE[L] and SWEDEN[L]	read	4.5T+2	

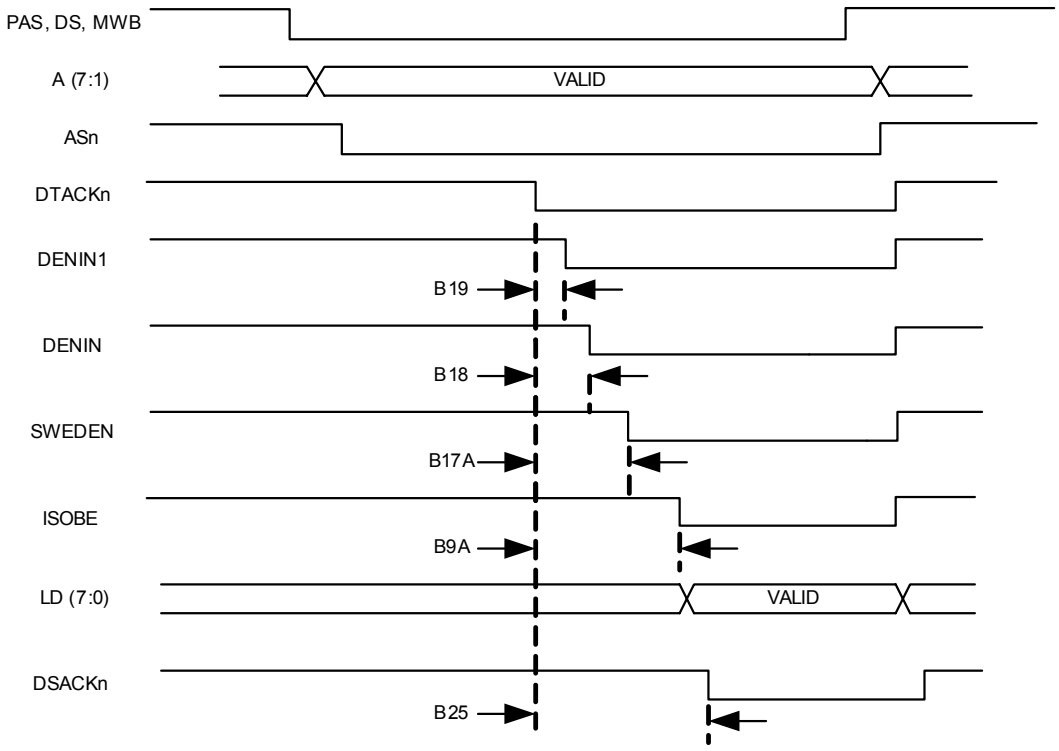

Fig. 1 VME Master Read

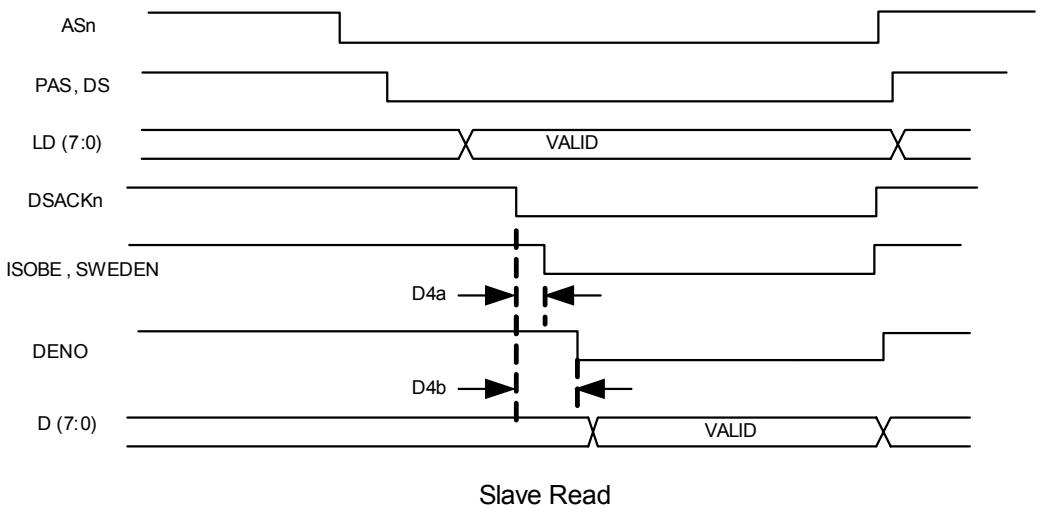

Fig. 2 Slave Read

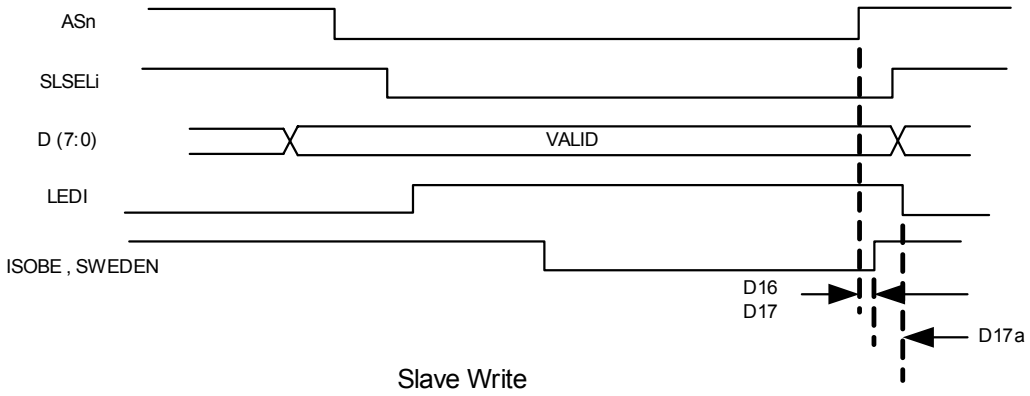

Fig. 3 Slave Write

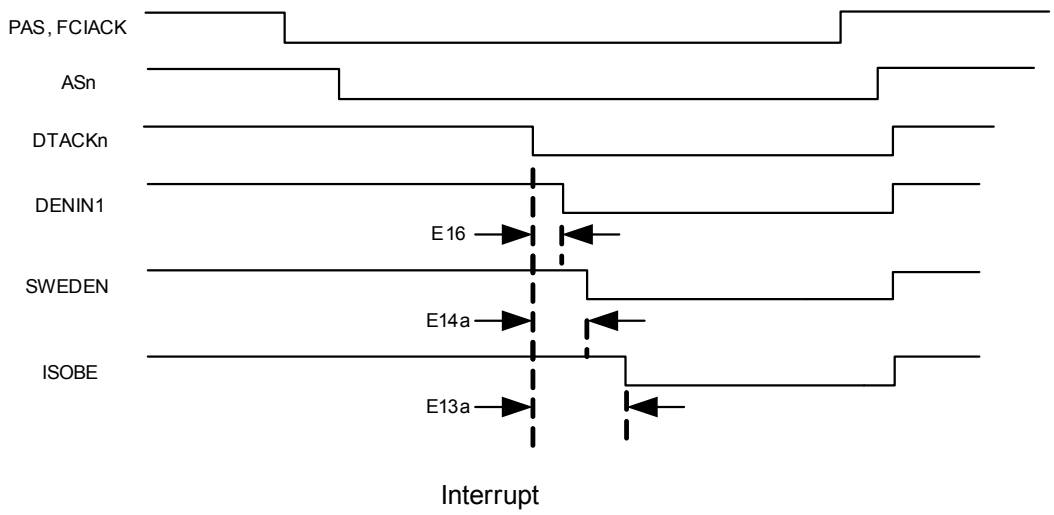

Fig. 4 FCIACK cycle

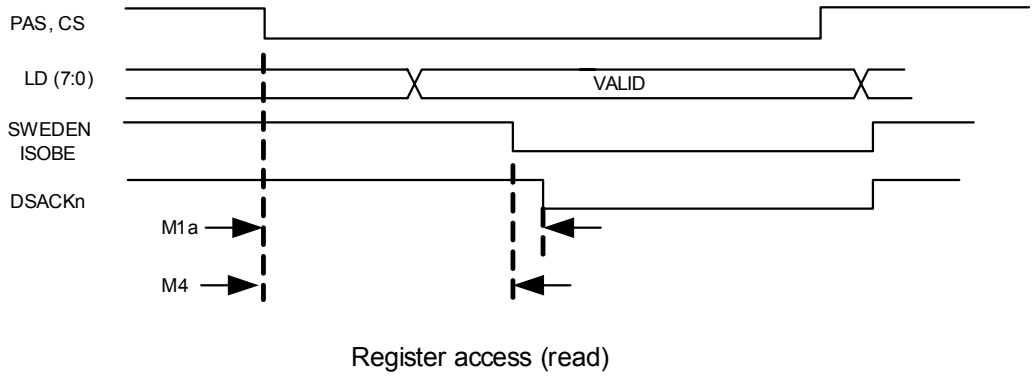

Fig. 5 Register Access read