ID MOS Digital I.P. SHORTFORM

IM109: High Level Data Link Controler

PRODUCT DESCRIPTION

This HDLC controller realises the interface between a Synchronous Serial Interface (SSI) and a microprocessor or DMA (Direct Memory Interface) interface.
It is compliant to the ECMA-40 (European Computer Manufacturers Association : HDLC frame structure) nd to others standard derivatives (CCITT X.25 (International Consultative Committee for Telegraphy and Telephony), ISO 3309-1979 (International Standard Organisation)…).

The controller does not manage the verification and the generation of the address field.

FEATURES

- 8 bit data bus width
- 8-bit data microprocessor interface
- flag number programmable from 1 to 4 in transmission mode
- bit-stuffing for transparency
- Cyclic Redundancy check (16-bit Frame Check Sequence)
- 6 modes : Transmission only, Reception only, full-duplex communication, loopback, transparent, loopback + transparent

BLOCK DESCRIPTION